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Sheet 1 of 1.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION  (Use several sheets if necessary)				Docket Number (Optional) YOR9200010217US2	Application Number 1692065 Not yet assigned		
				Applicant Magerlein et al.			
				Filing Date Concurrently herewith	Group Art Unit Not yet assigned		
<b>U. S. PATENT DOCUMENTS</b>							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
<i>DR</i>	6,339,024	1/15/02	Petrarca et al.	438	686	<i>/</i>	
<i>DR</i>	6,344,125	2/5/02	Locke et al.	205	118	<i>/</i>	
<i>DR</i>	6,368,484	4/9/02	Volant et al.	205	220	<i>/</i>	
<i>DR</i>	6,137,185	10-2002	Ishino et al.	257	786	<i>/</i>	
<i>DR</i>	6,373,273	04-2002	Akram et al.	324	765	<i>/</i>	
<i>DR</i>	5,808,360	09-1998	Akram et al.	257	738	<i>/</i>	
<b>FOREIGN PATENT DOCUMENTS</b>							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO
<b>OTHER DOCUMENTS</b> (including Author, Title, Date, Pertinent Pages, Etc.)							
<i>DR</i>	Richard Volant, Kevin Petrarca, Peter Locke, James A. Tornello and Donald F. Canapeni, Title: <i>"Replated Metal Structures for Semiconductor Devices"</i> , U.S. Patent application Serial No. 09/657,469, filed on May 9, 2000.						
EXAMINER				DATE CONSIDERED <i>7/28/04</i>			
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